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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/416,700	10/12/1999	ERIC SWANSON	HCAI-245.805	6494

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EXAMINER	
NGUYEN, TANH Q	

ART UNIT	PAPER NUMBER
2182	9

DATE MAILED: 07/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/416,700	SWANSON, ERIC	
	Examiner	Art Unit	
	Tanh Q. Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2002 and 19 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) *3-17,21-26,29-43 and 47-52* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,18-20,27,28 and 44-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Species I drawn to FIG. 21 (claims 1, 2, 18-20, 27, 28, 44-46) in Paper No. 5 and Paper No. 8 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 3-17, 21-26, 29-43 and 47-52 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5 and Paper No. 8.

Specification/Priority

3. An application in which the benefits of an earlier application are desired must contain a specific reference to the prior application(s) in the first sentence of the specification following the title of the invention, or in an application data sheet (37 CFR 1.78(a)(2) and (a)(5)).

The specific reference to the prior application(s) is **not** in the first sentence of the specification following the title of the invention. The Serial No. of a related application on page 2, line 3 of the "CROSS REFERENCE TO RELATED APPLICATION" is also missing. Appropriate correction is required.

Claim Objections

4. Claims 1, 2, 18 and 27, 28, 44 are objected to because of the following informalities:

Claim 1 recites both the limitations "first data domain" and "first domain" in lines 2-4. Consistency of terminology is recommended.

Claim 2 recites the limitation "the time domain" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim 18 recites the limitation "a second data rate" in line 3. This limitation implies that there is a first data rate - without a first data rate being recited.

Claim 27 recites both the limitations "first data domain" and "first domain" in lines 2-4. Consistency of terminology is recommended.

Claim 28 recites the limitation "the time domain" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 44 recites the limitation "a second data rate" in lines 2-3. This limitation implies that there is a first data rate - without a first data rate being recited.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by **Ioka (USP 5,745,190)**.

7. As per claim 1, **Ioka** teaches a method for collecting statistics on data (col. 4, lines 7-54) comprising the steps of:

analog data being converted by an A/D converter (col. 4, lines 15-22), hence the A/D converter receiving input data in a first data domain (analog domain) on an input of the A/D converter;

converting received input data with a data converter (A/D converter) from the first data domain to a second data domain (digital domain) different from the first data domain (col. 4, lines 15-22);

determining with a statistical processor [14, FIG. 1] statistical information (col. 4, lines 45-52) from the output of the data converter [50, FIG. 1]; and

allowing external access to the output of the statistical processor through an output interface [66, 16, FIG. 1].

8. As per claims 2, 18, Ioka teaches:

the analog data of video signals being converted to pixels that are scanned by the statistical processor sequentially (col. 4, lines 46-47; col. 4, lines 15-16), hence the step of converting operating in a time domain; and

the statistical processor scanning all pixels of the input frame from the data converter (col. 4, lines 46-47; col. 4, lines 15-16), and operating a mean value and a

standard deviation with respect to the input frame using all pixels of the input frame (col. 4, lines 45-52), hence the data converter providing data at a first sampling rate (pixels of the input frame), and the statistical processor providing an output at a data rate (mean value and standard deviation for the input frame) lower than the first sample rate.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ioka** in view of **Favreau (USP 4,317,129)**.

Ioka teaches the claimed invention except for the statistical processor being operable to operate on less than all data samples output by the data converter, wherein the less than all data samples comprises every jth sample, with j being greater than one.

Favreau teaches a logic gate [9, FIG. 1] for inhibiting data of one out of every two digital samples received from an A/D converter [3, FIG. 1] prior to transmitting to an output [8, FIG. 1] to obtain a good definition of signals without increasing bandwidth (col. 1, lines 12-22; col. 1, lines 44-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Ioka's statistical processor with one out of two digital samples, as is taught by Favreau, to allow Ioka's system to obtain a good definition of the data without increasing bandwidth.

11. Claims 27-28, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Intrater et al. (USP 5,630,153)** in view of **Ioka**.

12. As per claim 27, **Intrater et al.** (Intrater) teaches an integrated circuit (Rockwell Module: col. 2, lines 20-35), comprising:

an input [ANALOG CHANNEL, FIG. 1] for receiving input data in a first data domain (analog domain: col. 2, lines 22-25);

a data converter [ANALOG FRONT END, FIG. 1] for converting received input data from the first data domain to a second data domain (digital domain: col. 2, lines 26-27) different from the first data domain;

a digital signal processor [DSP, FIG. 1] for processing the output from the data converter (col. 2, lines 27-32); and

an output interface for allowing external access to the output of the DSP [FIG. 1; col. 2, lines 32-35 – an output interface is necessary on the integrated circuit for connecting to the GENERAL PURPOSE PROCESSOR, and thereby allowing access to the output of the DSP (on the integrated circuit) by the GENERAL PURPOSE PROCESSOR (external access)].

Intrater, therefore, teaches the claimed invention except for the DSP being a dedicated statistical processor. Intrater, however, teaches the integrated circuit being a special purpose integrated circuit that uses a dedicated DSP (fax DSP) to achieve very specific tasks (facsimile data recovery: col. 2, line 64-col. 3, line 4). Intrater, in essence, teaches that for a different specific application, an integrated circuit with a different dedicated DSP (DSP corresponding to the different specific application) is used.

Ioka teaches a statistical processor for determining statistical information from the output of a data converter (see rejections to claims 1-2 and 18 above).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a statistical processor, as is taught by Ioka, as the dedicated DSP in the configuration disclosed by Intrater to determine statistical information from the output of the data converter when a special purpose integrated circuit is desired, for use with statistical applications.

13. As per claims 28 and 44, Ioka teaches Ioka teaches the data converter operating in a time domain (col. 4, lines 46-47; col. 4, lines 15-16); and the data converter providing data at a first sampling rate (pixels of the input frame) and the statistical processor providing an output at a data rate (mean value and standard deviation for the input frame) lower than the first sample rate (col. 4, lines 45-52; col. 4, lines 15-16)

14. Claims 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Intrater et al.** in view of **Ioka**, and further in view of **Favreau**.

The combination of Intrater/Ioka teaches the claimed invention except for the statistical processor being operable to operate on less than all data samples output by the data converter, wherein the less than all data samples comprises every jth sample, with j being greater than one.

Favreau teaches a logic gate [9, FIG. 1] for inhibiting data of one out of every two digital samples received from an A/D converter [3, FIG. 1] prior to transmitting to an output [8, FIG. 1] to obtain a good definition of signals without increasing bandwidth (col. 1, lines 12-22; col. 1, lines 44-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the combination of Intrater/Ioka's statistical processor with one out of two digital samples, as is taught by Favreau, to allow Intrater/Ioka's system to obtain a good definition of the data without increasing bandwidth.

Double Patenting

15. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double

patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

16. Claims 1-2, 18 and 27-28, 44 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 18 and 21 of **U.S. Patent No. 6,369,738 (USP-738)** in view of **Ioka**.

17. As per claim 27, **USP-738** teaches a data converter (claim 15, line 1) comprising a self-contained integrated circuit (claim 21, lines 1-2), hence an integrated circuit comprising:

a time domain converter for receiving the analog input (claim 15, lines 3-4), hence an input for receiving input data in a first data domain (analog domain);

a data converter (time domain data converter) for converting received input data from the first data domain to a second data domain (digital domain) different from the first data domain (claim 15, lines 3-5);

a digital signal processor (frequency domain processor) for processing the output from the data converter (claim 15, lines 8-14); and

an output interface for allowing external access to the output of the digital signal processor (claim 15, lines 6-7; claim 18, lines 1-4).

USP-738, therefore, teaches the claimed invention except for the digital signal processor being a statistical processor. USP-738, however, teaches the integrated

circuit being a special purpose integrated circuit that uses a specific digital signal processor (frequency domain processor) to achieve specific tasks (tasks related time domain/frequency domain transform: claim 15, lines 8-14).

Ioka teaches a statistical processor for determining statistical information from the output of a data converter [14, FIG. 1].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a statistical processor, as is taught by Ioka, as the specific digital signal processor in the configuration disclosed by USP-738 to determine statistical information from the output of the data converter when a special purpose integrated circuit with statistical applications capabilities is desired.

18. As per claims 28, 44, Ioka teaches the data converter operating in a time domain (col. 4, lines 46-47; col. 4, lines 15-16); and the data converter providing data at a first sampling rate (pixels of the input frame) and the statistical processor providing an output at a data rate (mean value and standard deviation for the input frame) lower than the first sample rate (col. 4, lines 45-52; col. 4, lines 15-16). USP-738, further teaches a time domain converter (claim 15, line 3), hence the data converter operating in a time domain.

19. As per claims 1, 2, 18, USP-738, in combination with Ioka, teaches an integrated circuit for allowing external access to statistical information, hence teaches a method for collecting statistics on data with the integrated circuit.

20. Claims 19-20 and 45-46 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 18 and 21 of **U.S. Patent No. 6,369,738 (USP-738)** in view of **Ioka**, and further in view of **Favreau**.

The combination of USP-738/Ioka teaches the claimed invention except for the statistical processor being operable to operate on less than all data samples output by the data converter, wherein the less than all data samples comprises every jth sample, with j being greater than one.

Favreau teaches a logic gate [9, FIG. 1] for inhibiting data of one out of every two digital samples received from an A/D converter [3, FIG. 1] prior to transmitting to an output [8, FIG. 1] to obtain a good definition of signals without increasing bandwidth (col. 1, lines 12-22; col. 1, lines 44-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the combination of USP-738/Ioka's statistical processor with one out of two digital samples, as is taught by Favreau, to allow USP-738/Ioka's system to obtain a good definition of the data without increasing bandwidth.

21. Claims 1-2, 18 and 27-28, 44 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 - Paper No. 12 of copending **Application No. 09/376,761 (S/N 761)** in view of **Ioka**. This is a provisional obviousness-type double patenting rejection.

22. As per claim 27, **S/N 761** teaches an integrated circuit (line 1) comprising:

receiving a signal in the time domain (lines 1-2) and data from an analog format being converted by a data converter (lines 3-4), hence an input on the data converter for receiving input data in a first data domain (analog domain);

a data converter for converting received input data from the first data domain to a second data domain (digital domain) different from the first data domain (lines 3-4);

a digital signal processor (transform processor) for processing the output from the data converter (lines 7-9); and

an output interface from the integrated circuit (line 14), hence the output interface for allowing external access to the integrated circuit, the output interface allowing access to the output of the digital signal processor (lines 14-15).

S/N 761, therefore, teaches the claimed invention except for the digital signal processor being a statistical processor. S/N 761, however, teaches the integrated circuit being a special purpose integrated circuit that uses a specific digital signal processor (time domain/frequency domain transform processor) to achieve specific tasks (tasks related time domain/frequency domain transform: lines 7-9).

Ioka teaches a statistical processor for determining statistical information from the output of a data converter [14, FIG. 1].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a statistical processor, as is taught by Ioka, as the specific digital signal processor in the configuration disclosed by S/N 761 to determine statistical

information from the output of the data converter when a special purpose integrated circuit with statistical applications capabilities is desired.

23. As per claims 28, 44, Ioka teaches the data converter operating in a time domain (col. 4, lines 46-47; col. 4, lines 15-16); and the data converter providing data at a first sampling rate (pixels of the input frame) and the statistical processor providing an output at a data rate (mean value and standard deviation for the input frame) lower than the first sample rate (col. 4, lines 45-52; col. 4, lines 15-16). S/N 761 further teaches the data converter operating in a time domain (lines 3-4).

24. As per claims 1, 2, 18, S/N 761, in combination with Ioka, teaches an integrated circuit for allowing external access to statistical information, hence teaches a method for collecting statistics on data with the integrated circuit.

25. Claims 19-20 and 45-46 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 - Paper No. 12 of copending **Application No. 09/376,761 (S/N 761)** in view of **Ioka**, and further in view of **Favreau**.

The combination of S/N 761 and Ioka teaches the claimed invention except for the statistical processor being operable to operate on less than all data samples output by the data converter, wherein the less than all data samples comprises every jth sample, with j being greater than one.

Favreau teaches a logic gate [9, FIG. 1] for inhibiting data of one out of every two digital samples received from an A/D converter [3, FIG. 1] prior to transmitting to an output [8, FIG. 1] to obtain a good definition of signals without increasing bandwidth (col. 1, lines 12-22; col. 1, lines 44-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the combination of S/N 761 and Ioka's statistical processor with one out of two digital samples, as is taught by Favreau, to allow S/N 761 and Ioka's system to obtain a good definition of the data without increasing bandwidth.

Conclusion

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Quang Nguyen whose telephone number is (703) 305-0138, and whose e-mail address is tanh.nguyen36@uspto.gov. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin, can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7238 for After Final, (703) 746-7239 for Official, (703) 746-7240 for Customer Services, or (703) 746-5672 for Draft to the Examiner (please label "PROPOSED" or "DRAFT").

Any inquiry of a general nature relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Mail responses to this action should be sent to:

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Faxes for formal communications intended for entry should be sent to:

(703) 308-9051,

Hand-delivered responses should be brought to:

Crystal Park II, 2121 Crystal Drive, Arlington, Va, Fourth Floor

(Receptionist).

TQN

July 11, 2003